ABSTRACT

Off-chip driver (OCD) NMOS transistors with ESD protection are formed by interposing an P-ESD implant between the N+ drain regions of OCD NMOS transistors and the N-well such that the P-ESD surrounds a section of the N-well. The P-ESD implant is dosed less than the N+ source/drain implants but higher than the N-well dose. In another embodiment, N-well doping is used along with P-ESD doping, where the P-ESD doping is chosen such that it counterdopes the N-well underneath the N+ drains. The N-well, however, still maintains electrical connection to the N+ drains. This procedure creates a larger surface under the area where the junction breakdown occurs and an increased radius of curvature of the junction. The P-ESD implant is covered by N-type on three sides creating better parasitic bipolar transistor characteristics.

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